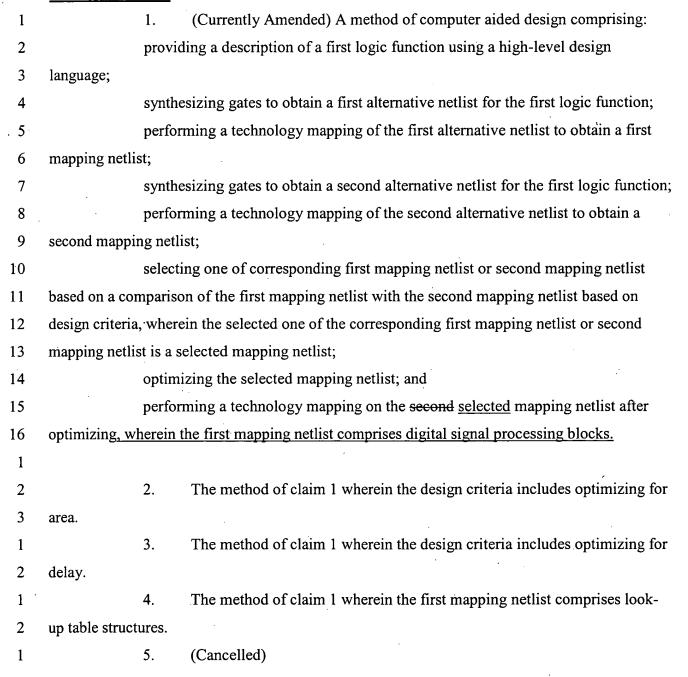
Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:



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1	6. The method of claim 1 wherein the first alternative netlist comprises lo	gic
2	gates.	
1	7. (Currently Amended) The method of claim 1 wherein the step of	
2	performing a technology mapping of the first alternative netlist to obtain a first mapping netlist	st is
3	done on a copy of the first alternative netlist.	
1	8. (Currently Amended) A method of logic synthesis comprising:	,
2	generating a first alternative netlist for a logic function;	
3	generating a second alternative netlist for the logic function, wherein the secon	ıd
4	alternative netlist has a different gate configuration from the first alternative netlist; and	
5	selecting one of the first <u>alternative netlist</u> or <u>the</u> second alternative netlists as a	a
5	selected alternative netlist based on results of a technology mapping of the first alternative net	tlist
7	and the second alternative netlists, wherein the first alternative netlist includes a digital signal	:
8	processing block.	
1	9. The method of claim 8 further comprising:	
2	performing a synthesis optimization on the selected alternative netlist to obtain	ı an
3	optimized selected alternative netlist.	
1	10. The method of claim 8 further comprising:	
2	performing a synthesis optimization on the selected alternative netlist to obtain	ı an
3	optimized selected alternative netlist; and	
4	performing a technology mapping on the optimized selected alternative netlist.	,
1	11. (Currently Amended) The method of claim 8 wherein the selecting one	of
2	the first <u>alternative netlist</u> or <u>the</u> second alternative netlists is based on area.	
1	12. (Currently Amended) The method of claim 8 wherein the selecting one	of
2	the first <u>alternative netlist</u> or <u>the</u> second alternative netlists is based on depth.	
1	13. (Currently Amended) A method of logic synthesis comprising:	
2	generating a netlist for a logic function;	
3	performing a first technology mapping on the netlist;	
4	after the first technology mapping, performing a synthesis optimization on the	
5	netlist; and	

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6	after the synthesis optimization, performing a second technology mapping on the
7	netlist, wherein the first technology mapping includes a digital signal processing block.

- 14. The method of claim 13 wherein the first technology mapping maps the netlist to the same target technology as the second technology mapping.
- 1 15. The method of claim 13 wherein the logic function is provided in a high-2 level design language.